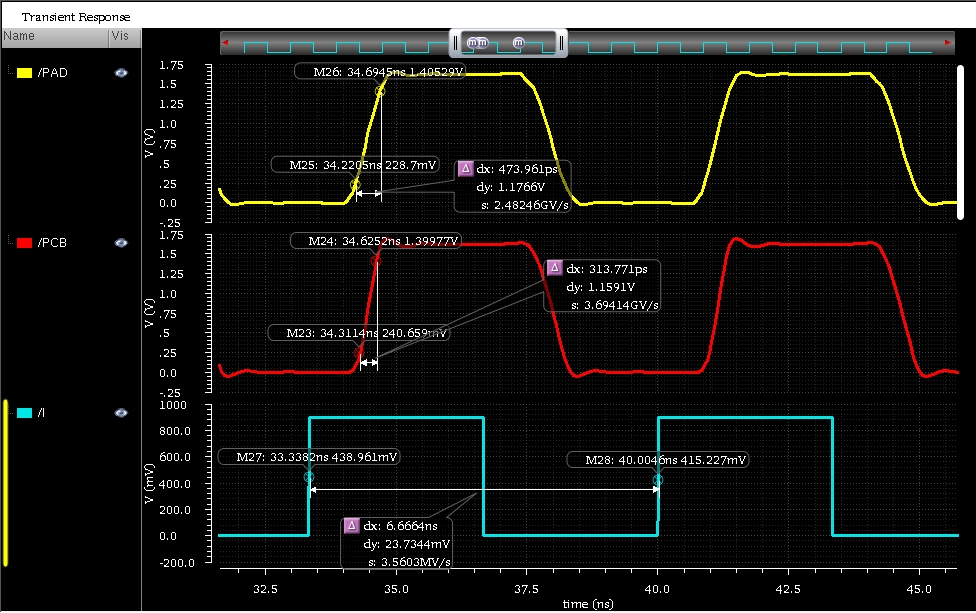
# 1.8V dig Pad Simulation

1.8V digital IO, loading 5-10pf, speed requirement 148.5MHz DDR:

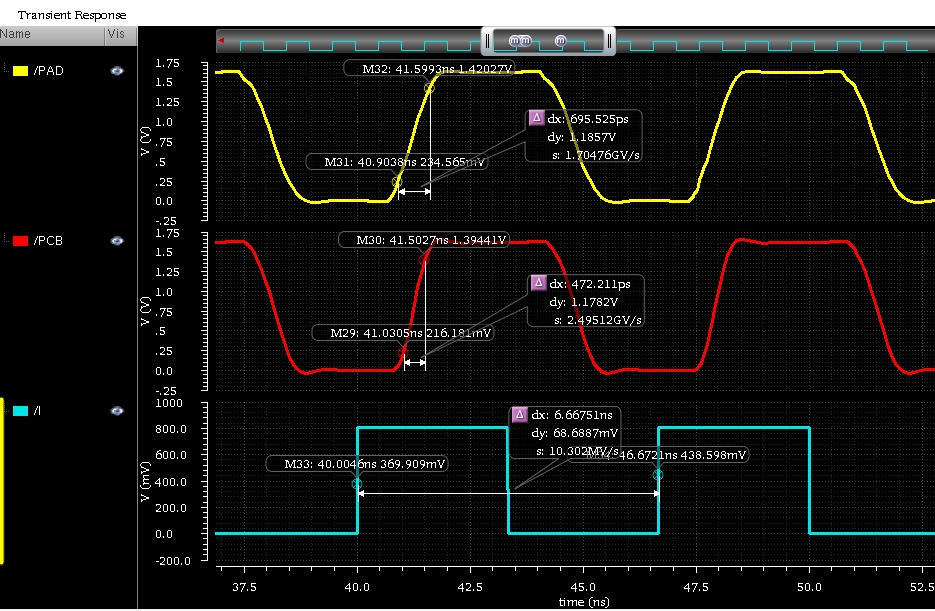
## 1 Set DS1, DS0 2’b11

150MHz clock ss corner LV/HT simulation result:

1. with 5pf



1. with 10pf



## 2. Set DS1, DS0 to 2’b00

150MHz clock ss corner LV/HT with 10pf simulation result as follows:

